JAMES COOLE

Raleigh, NC
james@coole.me

EXPERIENCE

Cisco June 2016 - Present
Technical Lead *Research Triangle Park, NC*

- Currently working on the Silicon One P4 compiler and toolchain. Work with the ASIC team and P4 application engineers to enable new hardware features, devices, device families, and applications; add optimizations to help dataplane code fit within device resources; and responsible for language evolution.
- Previously worked on P4 SmartNICs in the Data Center CTO and CTAO offices. Developed P4-to-RTL hardware compilers targeting FPGA, eFPGA + ASIC, and ASIC technologies. Included novel high-level optimizations and auto-pipelining driven by timing information extracted for each technology. Implemented as backends for ONF's P4-16 reference compiler, p4c.

University of Florida and NSF CHREC August 2009 - May 2016
Graduate Researcher/Fellow *Gainesville, FL*

- Researched *reconfiguration contexts*, an approach to FPGA high-level synthesis providing fast compilation and program portability that synthesizes kernel source at runtime using a library of pre-synthesized coarse-grained FPGA overlays. Developed enabling overlay architectures based on CGRAs and datapath merging, mapping and PnR algorithms for each, and tools to automatically design these overlays based on an analysis of expected kernels.
- Developed tools for FPGA high-level synthesis from OpenCL 1.1, based on Clang and LLVM, targeting libraries of reconfiguration contexts to provide $O(1s)$/kernel compile times. Included novel optimizations for OpenCL synthesis, including inference of sliding-window buffer hardware.
- Researched *block-based place and route*, fast PnR of high-level designs by assembling netlists from a library of pre-synthesized coarse-grained *blocks*. Developed a block-based variant of VPR and tools for generating these block libraries via floorplaning and manipulation of the vendor's full-detail PnR solutions. Involved reverse-engineering portions of the Altera Cyclone III's routing architecture.

NASA Goddard Space Flight Center May 2014 - May 2016
Computer Engineer *Greenbelt, MD*

- Extended OpenCL high-level synthesis tools I developed at UF with an implementation of the OpenCL runtime 1.1, including a Linux kernel module supporting often copy-less data movement to and from accelerators in Xilinx's Zynq family of SoCs and dynamic swapping of overlays.
- Integrated experiments using this framework into a CubeSat built on the Zynq-based CHREC Space Processor for an experimental mission on the International Space Station installed in 2017.
- Used this framework to implement several stages of a hyperspectral imaging application for real-time processing in satellite and UAV targets on a Zynq.

University of Florida August 2008 - August 2009
Research Assistant *Gainesville, FL*

- Researched *traversal caches*, a hardware/software framework that improves memory performance for data structures requiring non-sequential accesses (e.g. tree traversal). Used to develop efficient FPGA accelerators for 2 and 3D $n \log n$ (Barnes-Hut) n-body simulation.

Prioria, Inc. Summer 2008
Hardware Engineer Intern *Gainesville, FL*

- Helped design and implement a system for automated and interactive test of MRI RF coils. Implemented system control and hardware-accelerated DSP on a Cyclone II. Developed a control GUI in Cocoa for remote testing over ethernet.

EDUCATION

University of Florida *May 2016*
Ph.D. in Electrical & Computer Engineering
Thesis: *FPGA Overlays and Runtime Synthesis for Flexibility and Productivity*

University of Florida *May 2012*
M.S. in Electrical & Computer Engineering

University of Florida *May 2008*
B.S. in Computer Engineering, *Magna Cum Laude*

TECHNICAL STRENGTHS

Languages & APIs	C++, Python, P4-16, Verilog, LLVM
Hardware & Tools	Vivado, Quartus

SELECTED PUBLICATIONS AND PATENTS

- J. Coole and G. Stitt. Intermediate Fabrics: Virtual Architectures for Circuit Portability and Fast Placement and Routing. In *Proceedings of IEEE/ACM/IFIP Conference on Hardware/Software Codesign and System Synthesis*, CODES+ISSS, 2010.
- J. Coole and G. Stitt. Fast, Flexible High-Level Synthesis from OpenCL using Reconfiguration Contexts. *Micro, IEEE*, 34(1), Jan 2014.
- J. Coole and G. Stitt. Adjustable-Cost Overlays for Runtime Compilation. In *Field-Programmable Custom Computing Machines (FCCM), IEEE 23rd International Symposium on*, 2015.
- J. Coole and G. Stitt. BPR: Fast FPGA Placement and Routing Using Macroblocks. In *Proceedings of IEEE/ACM/IFIP Conference on Hardware/Software Codesign and System Synthesis*, CODES+ISSS, 2012.
- J. Coole and G. Stitt. OpenCL High-Level Synthesis for Mainstream FPGA Acceleration (*Invited Talk*). In *Workshop on SoCs, Heterogeneous Architectures and Workloads (SHAW)*, 2014.
- C. Wilson, J. Stewart, P. Gauvin, J. MacKinnon, J. Coole, J. Urriste, A. George, G. Crum, E. Timmons, J. Beck, et al. CSP hybrid space computing for STP-H5/ISEM on ISS. In *Proceedings of the AIAA/USU Conference on Small Satellites*, 2015.
- J. Coole, J. Wernsing, and G. Stitt. A Traversal Cache Framework for FPGA Acceleration of Pointer Data Structures: A Case Study on Barnes-Hut N-body Simulation. In *Proceedings of the International Conference on Reconfigurable Computing and FPGAs*, ReConFig, 2009.
- D. Wilson, G. Stitt, and J. Coole. A Recurrently Generated Overlay Architecture for Rapid FPGA Application Development. In *International Symposium on Highly-Efficient Accelerators & Reconfigurable Technologies*, 2018.
- J. Coole and G. Stitt. Overlay architecture for programming FPGAs, 2019. US Patent 10516396.
- J. Coole. Implementing configurable packet parsers for field-programmable gate arrays using hardened resources, 2021. US Patent 11095760.

PROFESSIONAL SERVICE

Program Committee Member, IEEE International Symposium On Field-Programmable Custom Computing Machines (FCCM), 2021-2023